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[20-HKPGDEO–M2S(O)21J]

MScIT/PGDCA/MCA 2nd Semester (Old) Exam., 2020

COMPUTER ORGANIZATION AND ARCHITECTURE

[MScIT/PGDCA/MCA (S2) 05]

Full Marks : 80

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. Answer any *five* of the following questions : 2×5=10

(a) What is hit ratio?

(b) Define interrupt nesting.

(c) What is an instruction cycle?

(d) What is universal serial bus? Mention the data transfer types of USB.

(e) What does a program counter do?

(f) Mention the properties of register transfer in I/O organization.

2. Answer any *three* of the following questions : 4×3=12

(a) Mention the basic difference between CISC and RISC. Also mention four characteristics of CISC.

(b) Give two examples each for accumulator organization, stack organization, general register organization instruction.

(c) Give Flynn's classification of parallel computer architecture.

(d) To address a word in the main memory, how many bit addresses are required for a computer having 4K main and 1K cache memory? Why is virtual memory necessary?

3. Answer any *three* of the following questions : 6×3=18

   (a) Explain the set associative mapping process. Also mention the disadvantage of direct mapping technique.

   (b) Briefly explain any one page replacement algorithm for efficient utilization of main memory space.

   (c) Explain the sequence of execution of the interrupt cycle.

   (d) Briefly discuss parallel computer architecture.

4. Answer any *four* of the following questions : 10×4=40

   (a) Write short notes on any *two* of the following : 5×2=10

      (i) Attached Array Processor

      (ii) Direct Memory Address (DMA)

      (iii) Pipelining

   (b) Elaborate on the different types of addressing modes. Give suitable examples for each of these types of addressing modes. 10

   (c) Write the working principle of auxiliary and associative memory. How does CPU connect the RAM and ROM chips? 6+4=10

   (d) What are the possible techniques for resolving a pipelining hazard? Describe any one hazard in pipelining in brief. 4+6=10

   (e) *(i)* Define RTL. Give four features of RTL. 5

      (ii) Describe the different types of shift registers. 5

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