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824 (COA)

[20-HKPGDEN-M2S(N)21J]

PGCA/ScIT/PGDCA 2nd Semester (New) Exam., 2020

COMPUTER ORGANIZATION AND ARCHITECTURE

[PGCA/ScIT/PGDCA-S2-01]

Full Marks : 80

Time : 3 hours

The figures in the margin indicate full marks for the questions

1. *(a)* Answer the following questions : 1×8=8

(i) Define bus.

(ii) Give two examples of two-address instruction.

(iii) Define memory-mapped I/O.

(iv) Define memory cycle time.

(v) Define universal serial bus.

(vi) Define auxiliary memory.

(vii) Define instruction register.

(viii) Write the main feature of EPROM.

(b) Choose the correct answer : 1×4=4

(i) The register that is used to keep track of next instruction to be executed is

(1) program counter

(2) instruction register

(3) program status word

(4) stack pointer

(ii) In Master-Slave flip-flop, the master changes state

(1) after the slave

(2) with the slave at the same time

(3) before the slave

(4) never

(iii) In which addressing mode, the operand is specified in the instruction itself?

(1) Direct

(2) Indirect

(3) Register

(4) Register indirect

(iv) The devices in _____ technique are connected in a serial manner.

(1) interrupt driven I/O

(2) daisy chaining

(3) handshaking

(4) None of the above

(c) Fill in the blanks : 1×4=4

(i) Control unit determines the sequence of _____.

(ii) Register indirect addressing is also called _____.

(iii) The time which is taken for the beginning of the sector to reach the head is called _____.

(iv) Hardwired control unit is used in _____ processor.

2. Answer any *five* from the following questions : 2×5=10

(a) Differentiate between DRAM and SRAM.

(b) Add (–20) and (–25) using 2's complement representation.

(c) Explain how a negative integer can be represented using 2's complement concept.

(d) Define I/O scheduling.

(e) Define paging.

(f) Define Reduced Instruction Set Computer (RISC).

3. Answer any *four* from the following questions : 3×4=12

(a) Explain indirect addressing with an example.

(b) Discuss the function of cache memory. Explain the terms 'cache hit' and 'cache miss'.

(c) Explain various phases of instruction cycle.

(d) In what situation parallel processing is used? Explain.

(e) Explain how pipelining can increase the performance of a system compared to a single-processor system.

4. Answer any *three* from the following questions : 6×3=18

(a) Differentiate between Hardwired control and Microprogrammed control units.

(b) In what situation Direct Memory Access (DMA) is used? Explain.

(c) Discuss physical memory and virtual memory. Differentiate between logical and physical addresses.

(d) Define RAID technology. Explain different levels of RAID.

5. Answer any *three* from the following questions : 8×3=24

(a) Explain the function of a 8-to-1 multiplexer.

(b) Explain different types of addressing modes giving examples.

(c) Explain various types of operations that the machine instruction should be able to carry out.

(d) Define polling. Explain the interrupt driven I/O technique along with a block diagram.

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