UNIT 2: DIGITAL COMPONENTS

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2.1 LEARNING OBJECTIVES

After going through this unit you will be able to:

- define combinational circuit and sequential circuit
- describe the working principle of Half-adder, Full-adder
- describe the working principle of Half-subtractor, Full-subtractor
- describe the working principle of Multiplexer, Demultiplexer
- describe the working principle of Encoder, Decoder
- describe the working principle of Flip-Flop, Register, Counter

2.2 INTRODUCTION

In the previous unit, we have discussed about the basic organization of the computer. In this unit, we will discuss the various combinational and sequential circuits to build your understanding on different digital components that are used in digital applications. A sound knowledge on these components will make you feel confident to understand the working principle of many digital devices in general and the computer system in particular. Combinational circuits, sequential circuits along with counters and registers are covered in detail in this unit. In this next unit, we will explore different data representation systems.

2.3 COMBINATIONAL CIRCUITS

To obtain a desired output according to a Boolean equation, various logic gates are often interconnected. These circuits are called combinational circuits. These are the combinations of different fundamental logic gates and hence the name Combinational Circuit. Its main characteristic is that the output is solely determined by the present inputs.

Inputs to a combinational circuit are given as either 0 or 1 and outputs are also available as either 0 or 1. In the process of designing a combinational circuit, first, a truth table is formed for the Boolean expression, that describes the combinational circuit. Next, the function is simplified and then the simplified function is implemented with gates to obtain the logic diagram of the combinational circuit. We may also obtain the Boolean expression from this logic diagram after determining the truth table.

2.3.1 Half-Adder

Half-adder is a circuit that can add two binary bits. Its outputs are SUM and CARRY. The following truth table shows the various combinations of inputs and the corresponding outputs of a half-adder. X & Y denote inputs and C & S denotes the two outputs CARRY & SUM.

Table 2.1: Truth Table for a Half-Adder

X	Y	CARRY (C)	SUM (S)
0	0	0	0
0	1	0	1 ($\overline{X}Y$)
1	0	0	1($X\overline{Y}$)
1	1	1 (XY)	0

The minterms for Sum and CARRY are shown in the bracket. The Sum-Of-Product equation for SUM is :

$$S = \overline{X}Y + X\overline{Y} \quad \ldots\ldots\ldots\ldots (1)$$
$$= X \oplus Y$$

Similarly, the SOP equation for the CARRY is:

$$C = XY \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Combining the logic circuits for equation (1) & (2) we get the circuit for Half-Adder as :



Figure 2.1: Half-Adder Circuit and Symbol

2.3.2 Full-Adder

Full-Adder is a logic circuit to add three binary bits. Its outputs are SUM and CARRY. In the following truth table X,Y,Z are inputs and Ć and Ś are CARRY & SUM.

Table 2.2: Truth Table for Full- Adder

X	Y	Z	CARRY (Ć)	SUM (Ś)
0	0	0	0	0
0	0	1	0	1 ($\overline{X}\ \overline{Y}$ Z)
0	1	0	0	1 ($\overline{X}$ Y $\overline{Z}$)
0	1	1	1 ($\overline{X}$ YZ)	0
1	0	0	0	1 (X $\overline{Y}\ \overline{Z}$)
1	0	1	1 (X $\overline{Y}$ Z)	0
1	1	0	1 (XY $\overline{Z}$)	0
1	1	1	1 (XYZ)	1 (XYZ)

The minterms are written in the brackets for each 1 output in the truth table. From these, the SOP equation for full summation can be written as:

$$\acute{S} = \overline{X}\ \overline{Y}Z + \overline{X}Y\overline{Z} + X\overline{Y}\ \overline{Z} + XYZ$$

$$= \overline{X}\ (\overline{Y}Z + Y\overline{Z}\ ) + X(\overline{Y}\ \overline{Z}\ + YZ\ )$$

$$= \overline{X}S + X\overline{S} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ (3)$$

Here, S is SUM of Half-Adder.

Again, SOP equation for Full–Adder CARRY is :

$$\acute{C} = \overline{X}YZ + X\overline{Y}Z + XY\overline{Z} + XYZ$$

$$= \overline{X}YZ + XYZ + X\overline{Y}Z + XY\overline{Z}$$

$$= (\overline{X} + X)YZ + X(\overline{Y}Z + Y\overline{Z}\ )$$

$$= YZ + XS$$

$$= C + XS \quad \ldots\ldots\ldots\ldots\ldots\ldots\ (4)$$

Here also, C means CARRY of half-adder and S means SUM of half-adder.

Now, using two half-adder circuits and one OR gate we can implement equation (3) and (4) to obtain a full-adder circuit as follows.

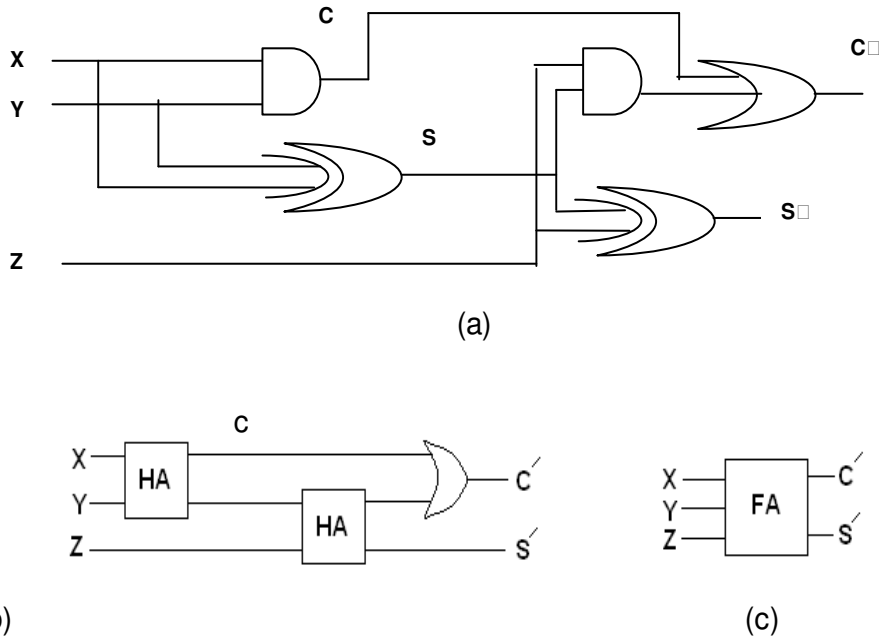


Figure 2.2: Full-Adder Circuit

(a) logic diagram, (b) block diagram (c) Symbol

2.3.3 Half - Subtractor

A half-subtractor subtracts one bit from another bit. It has two outputs, DIFFERENCE (D) and BORROW (B).

Table 2.3: Truth Table for Half-Subtractor

X	Y	BORROW(B)	DIFFERENCE (D)
0	0	0	0
0	1	1 ($\overline{X}$ Y)	1 ($\overline{X}$ Y)
1	0	0	1 (X $\overline{Y}$)
1	1	0	0

The mean terms are written within parenthesis for output 1 in each column. The SOP equations are :

$$D = \overline{X}Y + X\overline{Y} = X \oplus Y$$

$$= S \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

$$B = \overline{X}Y \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

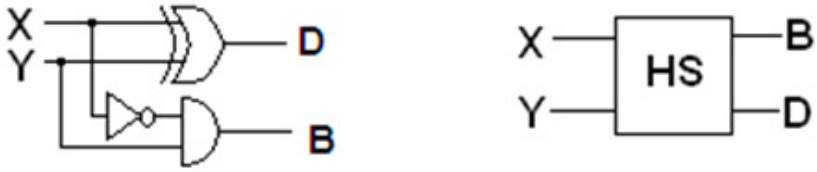


Figure 2.3: The Half-Subtractor circuit and symbol

2.3.4 Full-Subtractor

A full-subtractor circuit finds the Difference and Borrow on the subtraction operation involving three binary bits.

Table 2.4: Truth Table of Full-Subtractor

The SOP equation for the DIFFERENCE is :

$$D' = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ$$
$$= \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XYZ + \bar{X}\bar{Y}Z$$
$$= (\bar{X}Y + X\bar{Y})\bar{Z} + (XY + \bar{X}\bar{Y})Z$$
$$= D\bar{Z} + \bar{D}Z \quad \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

And SOP equation for BORROW is :

$$B' = \bar{X}\bar{Y}Z + \bar{X}Y\bar{Z} + \bar{X}YZ + XYZ$$
$$= \bar{X}\bar{Y}Z + XYZ + \bar{X}Y\bar{Z} + \bar{X}YZ$$
$$= (\bar{X}\bar{Y} + XY)Z + \bar{X}Y(\bar{Z} + Z)$$
$$= \bar{D}Z + \bar{X}Y \quad \ldots\ldots\ldots\ldots\ldots\ldots (8)$$